Parallel digital and symbolic optical computation via optical phase conjugation

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The use of the optical phase conjugation (OPC) process for parallel digital and symbolic optical computing is described. Using spatially encoded logic and symbolic variables, various OPC-based parallel ultrafast optical logic, symbolic as well as interconnect processors are detailed. The proposed devices are experimentally verified using picosecond pulses from a mode-locked Nd^{3+}:YAG laser. Based on these processors, an OPC-based ultrafast optical computing architecture is proposed.

I. Introduction

Nonlinear optical devices allow for the control of the frequency, direction, and amplitude of light through the use of another light beam.[1] Recent advances in the generation of picosecond and femtosecond optical pulses and in the identification of new optical materials has opened up the possibility of performing various signal and computational processing functions optically at very high data rates. An application of modern optical devices that requires both parallelism and ultrafast processing speed is digital computation. It is well known[2] that compared to analog processing, digital computations offer three major advantages: (1) it reduces cumulative noise; (2) it reduces approximation error; and (3) it leads to increased flexibility. A combination of these advantages together with ultrafast parallel processing properties of optics may lead to the realization of a digital optical computer. A number of nonlinear optical effects, such as the Kerr[3,4] and three- as well as four-wave mixing,[5-9] have been proposed for implementing optical digital computing elements.

In this paper, the use of a combination of optical phase conjugation (OPC) and parallel processing techniques to implement a number of fundamental logic, interconnect, as well as symbolic processors are discussed. Although these schemes can be implemented using a variety of slow speed photorefractive OPC

materials, using ultrafast third-order effect nonlinear materials, these processors will be able to manipulate data at a picosecond or subpicosecond rate.

The paper is organized as follows. In Sec. II, the use of OPC for the realization of binary and multiple-valued logic operations is described. In Sec. III, the core of an optical symbolic substitution processor (an OPC symbolic recognizer) is detailed. In Sec. IV, an OPC-based reconfigurable cross-bar interconnection element is described. In Sec. V, using these elemental OPC processors, both arithmetic and symbolic computing architectures are presented. In Sec. VI, experimental results obtained with 32-ps Nd^{3+}:YAG laser pulses are presented.

II. Parallel Optical Logic Using Optical Phase Conjugation

The nonlinear optical phase conjugation (OPC) effect offers solutions to many real-time optical signal and image processing problems. In an analog mode, OPC signals (images) can be processed in parallel.[10-13] In a digital mode, OPC logic implementations have been suggested. The optical logic variables can be represented both by the beam on/off[7] and by its orthogonal polarization[6] states. Using these representations, a number of binary optical logic elements, such as an AND, exclusive-OR (EOR), NOT, have been described. A shortcoming of these encoding approaches is that other useful binary logic operations are difficult to perform. Although either a NAND or NOR is sufficient to implement all binary operations, the availability of the other logic functions can increase the computer's processing speed and flexibility. It has been indicated that an encoding approach that uses orthogonal spatial patterns can lead to the optical implementations of all sixteen two-input binary logic operations. In a pattern logic encoding scheme,[14] the optical beam

passes through three consecutive, two input and an output, masks. This optical triple multiplication implies an optical triple-variable logic AND operation. By successively replacing the input and output masks, different logic functions can be generated. With this scheme the speed is limited to the time needed to physically create and change the masks. In this section, the use of the ultrafast OPC effect with a particular spatial pattern encoding method to perform all sixteen two-variable binary logic operations is described. This method will be extended to include optical multiple-valued logic implementations.

In Fig. 1, an OPC experimental setup is shown. Three input beams emanating from a common laser source, labeled E_A, E_B, and E_C, are collimated into a cubic $[\chi^{(3)}]$ nonlinear material (NLM). The beams E_A and E_B are mutually phase conjugate. The third, the off-axis operational kernel, beam E_C is the probe. The nonlinear interaction of the three beams in the NLM generates a polarization source that radiates a fourth beam $E_0 \propto \chi^3 E_A E_B E_C^*$, where the * stands for complex conjugation. The two input logic beams $E_A(E_B)$ are vertically (horizontally) encoded and are present at either half of the full aperture, while the third beam E_C, depending on the logic operations, can be located at the four available quadrants of the output aperture. When all three beams are present a phase conjugate output signal E_0 is generated. This signal, separated out by a beam splitter, is then detected by a four-quadrant detector. For the various logic operations, different operational kernels are used.[8]

This OPC-based logic processor can be modified to perform ultrafast multiple-valued logic operations. The preference for a multiple-valued logic system is mainly due to the fact that it can process more information (compared to its binary counterpart) through a unit interconnection at a unit time.[15] It has been noted[16] that for an input energy level encoding scheme, it is difficult to obtain a multiintensity level switch. However, it is relatively easy to encode the multiple levels into spatial locations. Shadow casting is one way to perform spatial multiple-valued logic operation.[17] Here, instead of dividing the aperture into two, as in the binary case, it is decomposed into multiple equal area sections. In Fig. 2, the spatial encoding for two ternary (quaternary) logic variables is shown. The superposition of the two patterns will address only one of nine (sixteen) possible spatial locations. For the different two-variable multiple-valued logic operations, again, various kernel operations are employed. Thus, using this encoding scheme and an OPC processor, real-time multiple-valued logic operations can be performed.

Using an OPC-based logic scheme, the advantages of both optical parallel and ultrafast processing can be realized. For example, for an OPC channel area of 50 $\times$ 50 μm^2 (an integrated optics scale), a 2- $\times$ 2-cm^2 OPC aperture will contain 1.6 $\times$ 10^5 2-D spatial channels. An expanded beam of a commercial 30-ps pulse mode-locked Nd^{3+}:YAG laser delivering 60-mJ energy to such area can yield a power density of 50 MW/cm^2.
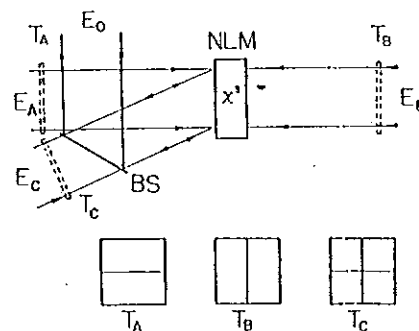

Fig. 1. OPC-based optical binary logic processor: NLM, nonlinear material; $T_{A(B)}$, two spatially encoded logic masks for logic variables $A(B)$; T_C, an operational kernel mask.
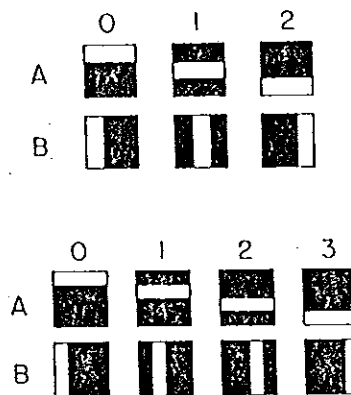

Fig. 2. Two-variable ternary and quarternary spatial logic encoding examples.

With this power density and CS$_2$ as the NLM, OPC signals over the whole aperture can be generated. Using a femtosecond mode-locked dye laser, an even larger power density and high repetition rate (200 MHz) can be obtained. With such a source, an OPC processor may perform about 10^{13} logic operations per second.

III. Optical Phase-Conjugation-Based Symbolic Pattern Recognition

Recently, optical symbolic substitution (OSS) as a computation scheme has been introduced.[18] Instead of decomposing computation into stages of Boolean logic operations that use multiple inputs to generate a single output, the OSS scheme uses both multiple inputs and their relative locations to generate, in parallel, multiple spatial outputs. For an OSS, two (a recognition and a scription) suboperations are needed. For symbolic recognition, a device that performs spatial pattern shifts, collinear superposition (a logic OR), parallel NOR, and masking (a logic AND) operations was suggested. It has been indicated that recognition can also be performed using spatial shifts together with parallel AND operations only.[19] In this section, using an OPC device a shift and AND operation-based symbolic recognizer is described.

The symbolic pattern to be recognized consists of several elemental patterns within a large 2-D array of rectangular pixels. Although there are many possible
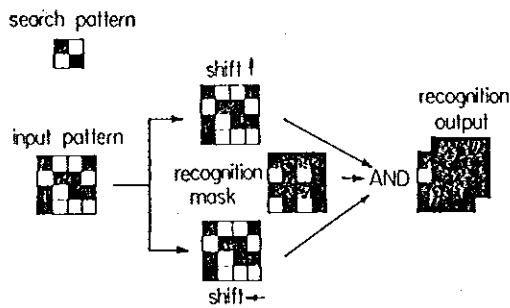
Fig. 3. AND operation-based symbolic pattern recognition example. To search for the upper left-hand side corner pattern, the input image is duplicated into two with one up- and the other left-shifted copies. Together with a recognition mask, the two shifted inputs are directed to a three-input parallel AND gate to generate the output shown at the right-hand side of the figure.

elemental pattern definitions, in this paper a four square-pixel intensity transparent/opaque code elemental pattern is considered. As an example, in Fig. 3, using the shift/AND scheme, the recognition of one such elemental pattern is considered. Here the input image consists of four different elemental patterns from which only the upper left elemental pattern needs to be recognized. For this task, the input is optically duplicated into two copies; then one copy is spatially shifted to the left, while the other is shifted downward. The two shifted copies together with the recognition mask input are then directed to a three-input parallel AND device that generates the final recognition result.

Since an OPC can be considered as a three-input AND element, to recognize an elemental pattern, in Fig. 4, a collimated input image beam is first divided by a beam splitter into two copies. Guided by two plane mirrors, the two beams counterpropagate with a relative spatial shift to a NLM. A third beam encoded with the recognition mask is also directed to the NLM. The thus generated OPC signal counterpropagates with respect to the third beam. Finally, using a second beam splitter, this signal is directed to the system output. Two advantages of this OPC-based approach are: (1) instead of three consecutive, an OR, a NOT, and an AND, only a triple-input AND operation is required; and (2) compared to a threshold-based symbolic operation, the use of an OPC-based AND element will reduce the cumulative error.

IV. Optical Phase Conjugation-based Reconfigurable Interconnect

In the previous sections, an OPC-based parallel logic and symbolic processing have been described. To perform multistage computation, the output of one processor needs to be distributed to one or many subsequent processors. For fast parallel computation, both fast logic (symbolic) processors and parallel data distribution (interconnection) schemes are required. One suggested digital optical interconnect method uses an array of holograms.[20] Each hologram is optimized for a different diffraction angle. Since for a given interconnect an array of fixed holograms is em-
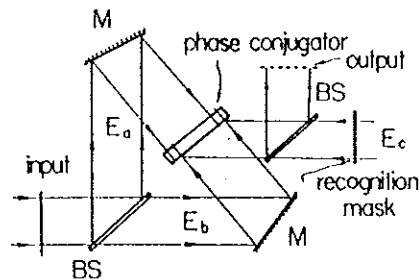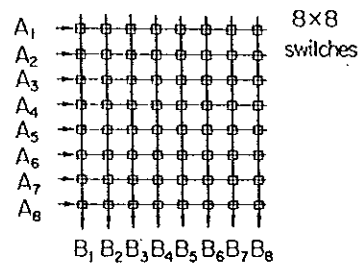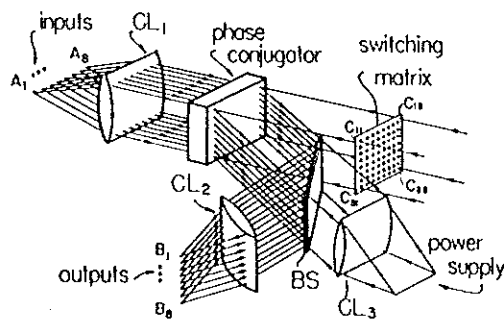

Fig. 4. Schematic of an OPC symbolic recognizer implementation. The input pattern duplication and spatial shifts are performed by a beam splitter (BS) and two mirrors. The recognition mask is inserted in the third beam. Using a second BS to the output, the recognized pattern is directed.

(a)

(b)

Fig. 5. (a) A schematic of an 8 × 8 crossbar interconnect. (b) An OPC-based optical implementation. Eight vertical light bars formed by an input cylindrical lens and an array of 8 × 8 switching beams are directed from the opposite side to the OPC cell. On OPC reflection of the third input, the output is separated by a BS and a second cylindrical lens to eight output channels.

ployed, for the various interconnections, a large set of hologram arrays together with some optical multiplexing scheme must be employed. To reduce the heavy memory space burden and adapt to the changing computational requirements, an optical dynamic interconnect device is needed. It has been indicated that one way to implement a reconfigurable interconnect is to use an electronically controlled optical crossbar switch.[21] An $N \times N$ crossbar links N input and output signal channels so that a change in one will not affect other links [see Fig. 5(a)]. To implement an optical free-space propagation mode crossbar switch, N input and output beam channels are 1-D spatially expanded with an input and output cylindrical lens to form per-

pendicular light-bar arrays that illuminate from two sides to a 2-D $N \times N$ switch array. Such an electrooptical (EO) deformable-mirror-based optical crossbar switch has been constructed.[21] Since the mirrors must mechanically deform, its switching speed is limited. Also, with an EO approach, electronic rather than optical signals are used to control optical beam deflections. Next, an OPC-based all-optical crossbar switch scheme is described.

In Fig. 5(b), an OPC parallel crossbar device is shown. As an example, an $N = 8$ switching array with eight input $(A_1, . . ., A_8)$ and output $(B_1, . . ., B_8)$ channels is depicted. The input beams to be incident on a NLM are vertically expanded into eight light bars. An 8×8 switching matrix beam array is also directed to the other side of NLM. The third input beam serves as an optical power supply. For example, to switch the signal from port A_1 to B_8, only one switching beam, located at the lower left corner of the switch array, needs to be on while all the other sixty-three beams are off. Correspondingly, the OPC signal will be guided through the output beam splitter and cylindrical lens to the output port B_8. As a second example, consider switching all eight input port $A_1, . . ., A_8$ signals to a single output port B_8. In this case, when all the inputs together with all the eight bottom switching beams, i.e., $C_{8,1}, . . ., C_{8,8}$, are on the eight output beams will be guided via the cylindrical lens to port B_8. Using this device, an OPC-based perfect shuffle can also be achieved. To perform this task, the switching beams $C_{1,1}, C_{2,3}, C_{3,5}, C_{4,7}, C_{5,2}, C_{6,4}$, and $C_{7,6}$ need to be activated.

Compared to existing schemes, the major advantage of an OPC-based approach is that an all-optical fast reconfigurable interconnect can be realized. In addition, by interchanging the optical power supply with the input channel ports, the input and output functions can be interchanged leading to a two-way optical crossbar interconnect.

V. OPC-Based Optical Computing Architecture

In this section, based on the previously discussed OPC logic, symbolic processing units as well as the interconnection scheme, an OPC-based optical computing architecture is proposed.

The key to the multistage operation of an OPC logic unit is its input/output encoding. For a fast operation, in addition to fast gates, a fast input/output modulation scheme must also be incorporated. Since for each of the two binary values, only half of the beam aperture is used, the initial input modulation can be performed using a fast EO deflector (see Fig. 6). In fact, using a waveguide structure, a two-level EO deflector can operate at a subnanosecond speed.[22] To increase further the deflection speed, an all-optical deflector is needed. Among the various ultrafast switching schemes, a nonlinear femtosecond response dynamic grating[23] may be helpful.

To convert a logic output to its next stage binary input, an optical 4×4 crossbar can be used. Now, instead of entering an operation kernel input for a
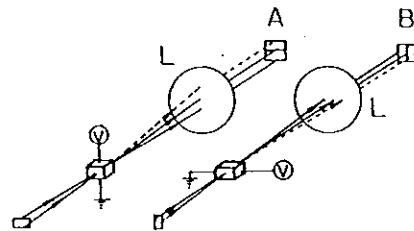

Fig. 6. Possible real-time binary input modulation scheme. Using a fast voltage controlled optical deflector and a lens, the optical signal can be switched to one of the two binary spatial locations.
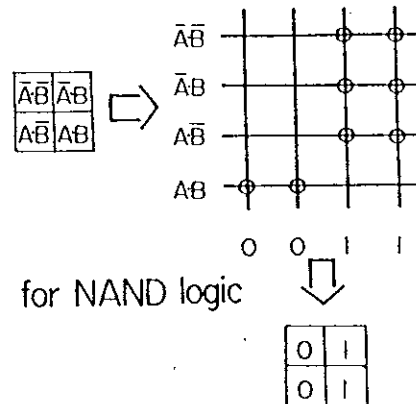

for NAND logic

Fig. 7. OPC interconnect for real-time spatially encoded optical NAND operation. Three of the four input channels representing $\overline{A}\overline{B}$, $\overline{A}B$, and $A\overline{B}$ are routed into two output channels representing a logic one, while the remaining AB is routed into the logic zero channels.
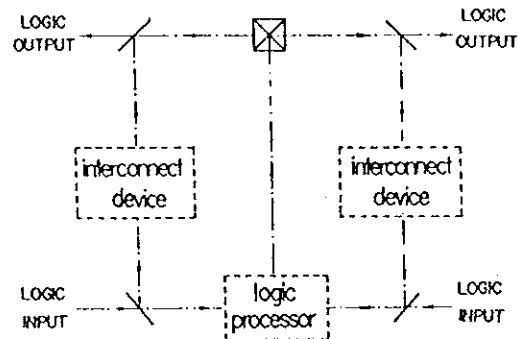

Fig. 8. OPC-based optical iterative processor. The system input (output) ports are located at the bottom (top) part of the processor. In addition to OPC logic units, for data permutation, two interconnect devices are used.

given logic function, the four OPC output quarters are directed to four crossbar input ports. As an example, consider the implementation of an NAND function (see Fig. 7). Each of the three, $\overline{A}\overline{B}$, $A\overline{B}$, and $\overline{A}B$, input channels is guided into two output channels representing a logic 1. On the other hand, the input channel AB is connected to the two 0 output channels. This output is suitable for further logic processing. Using this method, all the remaining two-variable logic functions can also be realized.

Based on this input/output encoding and logic processing, next, in Fig. 8, a schematic OPC-based iterative processing computer architecture is depicted.

The system contains three, i.e., one for logic and two for interconnection, elements. Inputs enter from the bottom sides of the processor. The parallel OPC outputs then pass through the first interconnect element to generate the first step cascadable logic outputs. For permutation, with lenses, beam splitters, and mirrors, these outputs are guided to the two interconnect devices. The permuted data together with new initial inputs can then be directed to the OPC cell etc. The final results are taken from the top sides of the processor. Assuming that each of the four OPC processor arms is 1 cm long and each NLM element has a 10-ps relaxation time, then, each computing iteration takes ~170 ps. With an integrated optics scale, further iteration speed increase is possible.

Using this architecture, both optical arithmetic and symbolic computation can be performed. As an example, consider the optical addition of two N-bit binary numbers. To generate with a full adder the sum and carry bit, four EOR and three AND gates are needed. When each gate uses two input channels at a time, with this approach, to add two 1-bit numbers, at least three parallel steps must be implemented. Correspondingly, the addition of two N-bit numbers results in $3N$ gate delay time. Obviously, this approach is time-consuming. It can be shown that an addition algorithm that uses a recursive array of half-adders (two-input EOR and AND gates) is less time-consuming. At each recursion step, a parallel bitwise sum and carry are generated. In the next recursion step, the one position left-shifted carry bits together with sum bits are used to produce the next step sum and carry bits. This process continues until all the carry bits become zero. The algorithm can be implemented with an OPC iterative processor. For example, to add the two 4-bit numbers $A = 1101$ and $B = 0111$, consider the OPC computational flow diagram shown in Fig. 9. The inputs enter from the right-hand side. The center kernel masks represent the required parallel EOR and AND operations. For the next stage processing, using two separate crossbar interconnects, the shuffled data are again fed back to the logic processor. In the top and bottom boxes in Fig. 9, the corresponding switching matrices for the required interconnects are shown. For this example, after three recursion steps (for the geometry described above it is ~0.6 ns), the summation result $S = 10100$ will be obtained.

In addition to arithmetic operation, the proposed OPC iterative processor can also be used to perform symbolic computing. As mentioned previously, symbolic computing is divided into two parts, a symbolic recognition and scription. While in Sec. III, an OPC symbolic recognizer was described; here an OPC symbolic scription oepration is given. Since the symbolic scription is a pattern duplication process, it can be implemented via an interconnect processor. In Fig. 10, a crossbar-based symbolic scription example is shown. Here the inputs and outputs of an 8 × 8 crossbar are connected to the inputs of two 4-pixel elemental symbolic patterns. For the given input patterns (see left-hand side of Fig. 10) and interconnec-
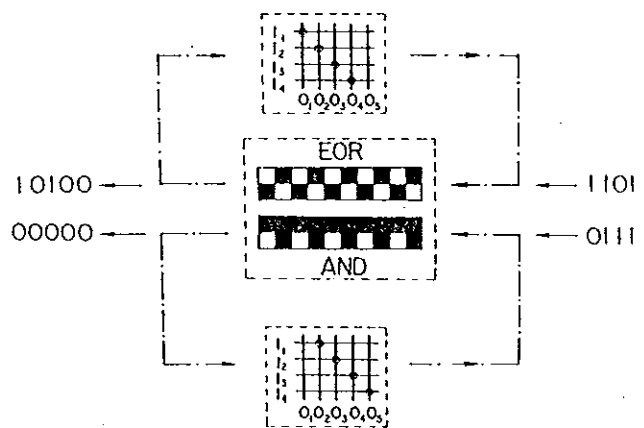

Fig. 9. OPC-based optical 4-bit addition example. Using an OPC half-adder (EOR and AND elements) array and two parallel interconnect devices, after three iterations, the summation output is generated.
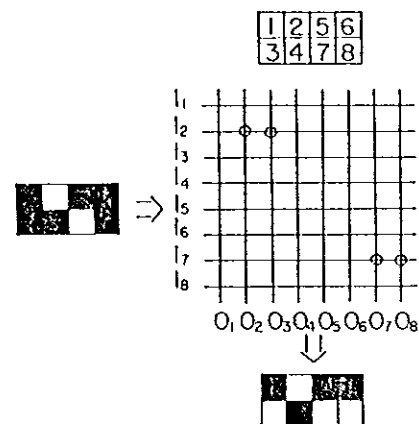

Fig. 10. OPC-based optical symbolic scription example. With the circled interconnects, at the output side, the two scripted output patterns are shown.

tion matrix (see center portion of Fig. 10), at the bottom of Fig. 10, the scription outputs are shown. Thus, using a parallel OPC-based pattern recognizer and crossbar scription together with feedback loops, programmable multistep symbolic substitution operations can be performed.

A practical OPC-based computing issue is signal fan-out. With most known ultrafast NLMs, the strength of the nonlinearity is limited. As a result, the OPC output attenuates relative in its input. To increase the OPC output power, two amplification approaches can be pursued. In a direct approach, a beam interaction length increase is utilized. Here, with a collinear geometry, the two counterpropagating inputs are identically polarized. Using a polarizing beam splitter, the orthogonally polarized third input beam is also directed to the NLM. As a source of nonlinearity,[24] instead of χ_{xxxx}, the χ_{yxxy} term is used. Usually, the value of χ_{yxxy} is smaller than that of χ_{xxxx}. For example, the ratio χ_{yxxy}/χ_{xxxx} is CS_2 is 0.7. However, this decrease can be compensated by an increase of the interaction length. The polarization of the OPC out-
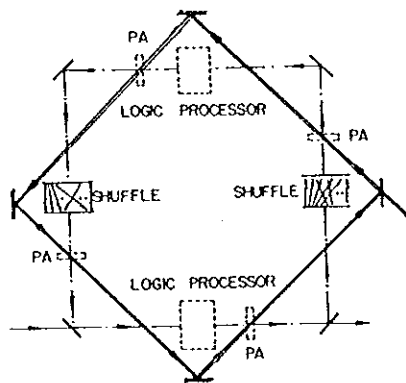
Fig. 11. Signal restoration scheme for an OPC iterative processor. At each processing arm, a parametric amplifier is placed. To synchronize, the strong pump beam must form an identical size beam loop.

Fig. 12. Picosecond OPC experimental arrangement. Using a beam expander (BE), a beam splitter BS_1, and two mirrors $M_{1(2)}$, the two derived beams are guided with ~10° separation to a CS_2 cell. To retroreflect the beam A, an end mirror M_3 is used. Three masks mounted on translational stages was also inserted. The OPC signal is directed by BS_2 to a recording camera.

put is parallel to the third input and can be separated by a polarizing beam splitter. Since this amplification scheme requires a longer pulse duration (in nanoseconds), its switching speed is rather slow. In an indirect (a parametric) amplification approach, a strong external laser pump pulse ω_3 is used to deliver optical power to the weak signal beam ω_1. When the signal and pump beams are mixed in an appropriate phase-matching geometry in a second-order nonlinear material, due to a nonlinear wave coupling, the weak signal is amplified. This parametric amplification scheme is widely used when a substantial laser power at a certain wavelength is required. Since some crystals provide a large gain (e.g., with NPP[25] a gain of $G = 10^4$ has been observed), the restoration of a weak OPC output to its original strength can be achieved. Recently, using a piece of 1.5-mm thick NPP organic crystal, the parametric amplification of a subpicosecond dye laser pulse has experimentally been demonstrated.[25] In Fig. 11, a possible schematic OPC signal restoration scheme is sketched. In a square-loop OPC processor, a second identical size loop is formed. Because of their identical size, the pulses traversing the two loops can be synchronized. For amplification, at each arm a parametric amplification cell is inserted. Due to their electronic nonlinearities, these cells do not absorb an appreciable amount of power, and, therefore, pump beam power can reused. Thus, using this amplification scheme at each OPC step, iterative computations are possible.

VI. Experiments

To verify the various proposed OPC-based digital processing concepts, a QUANTEL mode-locked Nd^{3+}:YAG laser that generates 32-ps optical pulses at 1064 nm was used in a number of preliminary experiments. In Fig. 12, the experimental setup is shown. First, using a KDP second harmonic crystal, the output pulse wavelength was converted from 1064 to 532 nm. To expand the beam spatial profile to a circular area of 2 cm², a 2× telescope was employed. Out of the expanded beam, a small portion (~1 cm²) was used.
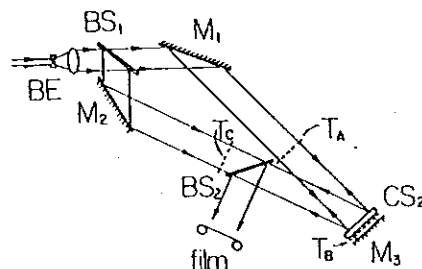
For a larger aperture parallel processing experiment, before the beam expansion, the pulsed source needs to be spatially filtered. The spatially expanded laser beam was divided using a 30/70 (reflection/transmission) ratio beam splitter into two parts denoted A and B. Beam A directed perpendicularly into a 2-mm thick CS_2 (2-ps response) cell, was reflected by a retroreflecting plane mirror located 2 mm behind the cell to form a counterpropagating beam geometry. Beam B passing through a second (with an equal splitting ratio) beam splitter was also guided from an off-axis direction (~5°) into the CS_2 cell. The counterpropagating OPC signal was directed by the second beam splitter to an output port. At this point, a camera was placed. Although a much better real-time input modulation scheme can be incorporated, in our preliminary experiment, binary masks mounted on translational stages were employed.

Using the above experimental arrangement, all sixteen binary two-variable logic operations were first performed. Two orthogonally encoded logic masks T_A and T_B were placed on the beam A at the front and back of the CS_2 cell, while all sixteen binary kernel masks mounted on a translational stage were inserted into beam B. To provide the appropriate spatial shifts, the translational stages were synchronously controlled. As the results corresponding to all sixteen logic operations, at the bottom of Fig. 13, the recorded light patterns are presented. To perform multiple-valued logic operations, the masks were modified. For a 2-bit ternary to binary conversion experiment, on the left-hand side of Fig. 14, the logic truth table as well as the input encoding scheme is shown. Since the output now contains 3 bits, three parallel OPC channels need to be used. In our experiment, the channel separation was performed by the translational stages. On the right-hand side of Fig. 14, the results of experimental conversion are illustrated.

The proposed OPC-based symbolic processor was verified next. An experimental sixteen-pixel input mask that contains four different four-pixel transparent/opaque elemental patterns (see top of Fig. 15) was used. To search for each of these patterns, an appropriate spatial shift and masking operation were incorporated (see middle of Fig. 15). With an appropriate
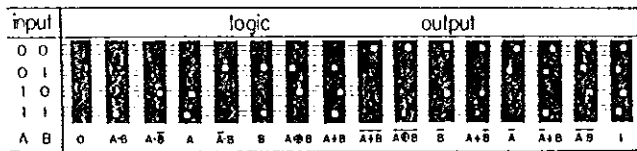
Fig. 13. (a) Input and operational kernel mask encoding schemes for sixteen two-variable binary logic operations. (b) The corresponding picosecond pulsed experimental results.
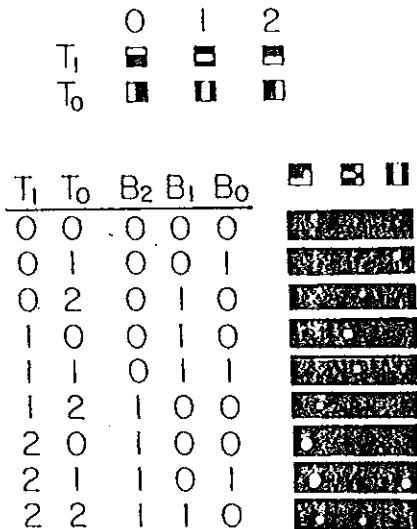

Fig. 14. Truth-table spatial encoding as well as the picosecond pulsed OPC experimental results for a 2-bit ternary-to-binary conversion operation.
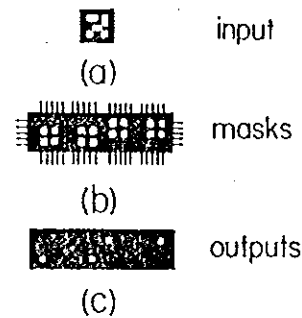

Fig. 15. Results of a picosecond OPC symbolic pattern recognition. (a) The input pattern contains four different four-pixel elemental patterns. (b) To recognize each elemental pattern, an appropriate spatial shift together with an appropriately positioned recognition mask is used. (c) The resulting four recognized patterns are shown.
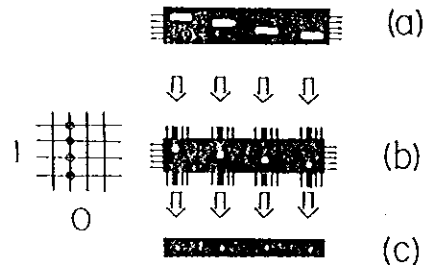

Fig. 16. Picosecond OPC-based 4 × 4 crossbar interconnect results. The routing of all four input to one, i.e., the third output channel: (a) input; (b) switching; (c) output light signals.
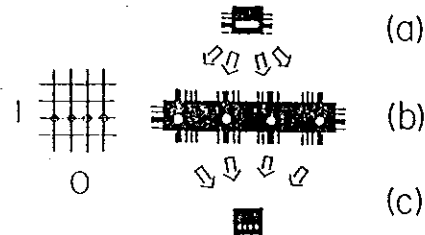

Fig. 17. Additional picosecond OPC-based 4 × 4 crossbar interconnect results. The routing of the third input to all four output channels is performed: (a) input; (b) switching; (c) output light signals.

spatial shift, the two beams containing two shifted copies of the input mask were directed from the opposite sides to the CS_2 cell. The probe beam B carried the recognition mask. As illustrated at the bottom of Fig. 15, the picosecond OPC output signals shows that the expected search patterns were located at the input image's lower left-, right-, upper left-, and right-hand side corners.

Finally, the experimental verification of an OPC-based 4 × 4 crossbar interconnection was performed. First, the routing of an input from each of the four input ports to a second output port was performed. Inputs were encoded as different level horizontal light bars to be incident on the NLM [see Fig. 16(a)]. In each case, in the second column, only one of the four switches was activated [see Fig. 16(b)]. In Fig. 16(c), the corresponding results are shown. In Fig. 17, using the OPC-based optical crossbar the results of routing of the signal from the third input to each of the four output ports were also demonstrated.

VII. Summary

An OPC device was used to perform various digital and symbolic optical computations. This device can be described as a four-port parallel optical AND processor. Using this processor, various digital optical binary and multiple-valued logic, symbolic, and interconnection operations were described. Using these processors, an OPC-based computation architecture has been proposed. A number of advantages are noted: (1) the use of OPC effect allows for parallel processing; (2) using fast optical nonlinear materials, such as the semiconductor-doped glasses, polymers, as well as multiple-quantum-well semiconductors, picosecond and sub-picosecond OPC switching can be obtained, and (3) since the OPC effect does not cause its output frequency shift, in principle, the proposed

schemes are cascadable. Experimental verification of some of the proposed operations using a mode-locked Nd^{3+}:YAG picosecond pulsed laser and CS_2 as the NLM were demonstrated. OPC-based multistage arithmetic and symbolic operations were also discussed.

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