
By John F. Wakerly.


Chapter 1  **Introduction**


Chapter 2  **Number System and Codes**

Omit sec. 7, 9, 16.2

Positional Number Systems. Various number systems and conversions between them, e.g. Bases 2, 8, 10, 16, BCD, 2’s Compliment.

Introduction to error detection and correction.

**HW:** p.74  Drill Problems – All

P.76  Exercises: 16, 18, 19, 24, 27, 33, 34, 38-41, 44-46, 50

Chapter 4  **Combinatorial Logic Design Principles**

Sum of product vs. Product of Sum Implementations. Static and Dynamic Hazards.

HW:   p.230 Drill Problems – All

Chapter 5  Hardware Description Languages
Sec 5.1, 5.3
HDL – Based Digital Design. Introduction to VDHL Hardware Description
HW:   p.337 Drill Problems – 3-5, 10
      p.338 Exercises 23, 26-31

Chapter 6  Combinatorial Logic Design Practices
Omit sections discussing ABEL and Verilog.
HW:   p.509 Drill Problems 1, 7, 13, 20, 21, 24, 30,
      p.511 Exercises 31, 36, 38, 43, 44, 46, 49, 51, 63, 70-72, 80, 82, 88, 101, 102.

Chapter 7  Sequential Logic Design Principles
Omit sec. 7.6, 7.9 – 7.11, 7.13
Latches and Flip Flops. Clocked Synchronous State Machine Analysis and Design. Sequential Circuit Design with VDHL.
HW:   p.664 Drill Problems – All
      p.669 Exercises 38, 41, 42, 46, 50, 55, 56, 59, 64, 65, 72, 77, 79, 87
Chapter 8  Sequential Design Practices
As time permits we will discuss Counters, Shift Registers and other practical concerns.

Chapter 9  Sequential Design Principles
As time permits.

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Course Requirements:  Percentage of Grade

• Midterms  TBD
• Final  TBD
• Several Programs  TBD
• One Breadboard Design  TBD

We will have several programming lab assignments in Assembly Language  and VHDL – in which case- the grading algorithm would be appropriately adjusted